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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,129	02/13/2002	Masahiro Sato	108075-00075	6390

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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,129	SATO ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8 and 10-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8 and 10-14* is/are rejected.

7)☒ Claim(s) *13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-8 and 10-14 are present in the application for reconsideration and have been examined. Claims 1, 5-8, 10 and 11 have been amended.

Claim Objections

2. Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In addition, base claims 11 and 12 must first be rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in ¶ 5 of this Office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 5, 6, 8, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al. (US-6587979), hereinafter Kraus in view of Takano (US-6097206), hereinafter Takano.

Claim 1:

Kraus teaches that the BIST circuit 7 (test circuit) communicates with a BIST controller circuit 8 (test device) which, as illustrated in FIG. 3A, may be implemented by a separate IC mounted on the same circuit board (load board 9) on which IC 2A is mounted when being tested by IC tester 5 (external test unit). (Col. 5, lines 20-24). Kraus also teaches the BIST circuit receives and stores data from the controller in the scan register. (Col. 3, lines 8, 9). Kraus discloses BIST circuit 11 includes a separate "core wrapper" 24 positioned near each RAM 12 which includes a scan register 46 for storing data, address and control signals appearing on bus 32 in response to the CAPTURE signal from tester 21 and shifts out its stored data onto the SHIFT_OUT line of scan bus 23 in response to successive pulses of the SHIFT signal from tester 21. (Col. 7, lines64, 65, Col. 11, lines 53-58). Kraus illustrates in FIG. 9 an embodiment of the test system including a load board 66 holding IC 10, a RAM 70 and a programmable BOST controller 71 clocked by a CLOCK signal from a source that may be internal or external to load board 66. Kraus teaches an external host computer 74 writes a test program into RAM 70 via conventional computer bus 76, and then sends a START command to BOST controller 71 via bus 76 telling it to execute that test program. Kraus also teaches the program stored in RAM 70 tells BOST controller 71 to carry out all test functions that might otherwise be carried out by tester 21 of FIG. 5 including supplying test pattern inputs to logic circuits 14, 16. Kraus further teaches a data comparator 52 which compares the data pattern generator 50 wrote into a RAM address to the data the RAM is currently reading back out of that address. When the RAM input and output data

fail to match, comparator 52 asserts the CERR signal (a decision circuit...determining the result). (Col. 12, ll. 12-28).

Kraus does not explicitly teach that the BOST includes a pattern generator...for providing previous stored second pattern data...". However, Kraus teaches RAM 70 of FIG. 9 may replaced with a read only memory (ROM) storing a test program (pattern data previously stored in the BOST device) appropriate for IC 10. (Col. 14, ll. 58-67, col. 15, ll. 1-5, 9-10). Kraus goes on to discloses an alternate embodiment in FIG. 10 of the test system similar to that of FIG. 9 except the BIST control functions are shared by an internal BIST controller 64 and external BOST controller 71. (Col. 15, ll. 16-20). Takano teaches in an analogous art a the memory testing apparatus 100 comprises a timing generator 20 for generating a reference clock (operating clock) which controls the operation of various parts or components, a pattern generator 11 for outputting address pattern data, test pattern data, expected value pattern data and the like, an address waveform generator 21 for generating an address pattern signal having a real waveform corresponding to an input address pattern data, a data waveform generator 22 for generating a test pattern signal having a real waveform corresponding to an input test pattern data, a driver 23 for applying the address pattern signal of real waveform generated from the address waveform generator 21 to an IC memory under test 200, a driver 24 for applying the test pattern signal of real waveform generated from the data waveform generator 22 to the IC memory under test 200, an analog comparator 25 for determining whether or not a response output signal read out of the IC memory under test 200 in the form of logic level has a given voltage value, a logical comparator 26 for

logically comparing data of the comparison result outputted from the analog comparator 25 with an expected value pattern data supplied from the pattern generator 11, and a failure analysis memory 27 for storing a failure data outputted from the logical comparator 26 each time both the data do not coincide with each other in the logical comparator, the failure data being stored in a memory cell of the failure analysis memory 27 at the address position specified by an address pattern data supplied from the pattern generator 11. (Col. 2, l. 45 to col. 3, l. 6). Takano also teaches in conjunction with the pattern generator 11 previously stored pattern data from the ROM expected value memory 16 is outputted during a timing test. (Col. 10, ll. 52-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kraus's BOST controller 71 to incorporate the pattern generating and previously stored pattern data functions of Takano's memory testing apparatus 100. The artisan would have been motivated to do so because it would enable Kraus to perform timing tests based on previously stored pattern data instead of newly generated pattern data or programs residing in the ROM.

Claim 3:

Kraus teaches an external host computer 74 (external test device) writes a test program into RAM 70 via conventional computer bus 76, and then sends a START command (control signal) to BOST controller 71 (BOST device) via bus 76 telling it to execute that test program. (Col. 14, lines 64-67, Col. 15, line 1)

Claim 5:

Kraus teaches a built-in self-test (BIST) circuit 11 incorporated into IC 10 for carrying out or facilitating any of several different types of tests on IC 10 (performing a pattern dependency test) including directly testing each RAM 12, and assisting in tests of logic circuits 14, 16. (Col. 6, lines, 47-51). Kraus also teaches when the core wrapper 24 (BIST circuit) detects a defective memory cell, it pulses an output current error signal (CERR). (Col. 11, lines 12-14). Kraus further teaches also teaches the BIST circuit 7 (BIST circuit) communicates with a BIST controller circuit 8 (BOST device). (Col. 5, lines 20-24).

Claim 6:

Kraus teaches In its "bit map" mode of operation, each core wrapper 24 (BOST device, see claim 11 rejection) loads test result data (reference data) for each addressable memory cell into its internal scan register so that tester 21 can acquire that data via scan bus 23 (provided to the external test unit). (Col. 10, lines 34-37).

Claim 8:

Kraus teaches BIST circuit 7 (semiconductor device) communicates with a BIST controller circuit 8 (BOST device) which, as illustrated in FIG. 3A, may be implemented by a separate IC mounted on the same circuit board (load board 9) (second contactor) on which IC 2A is mounted. Kraus further teaches an external BIST controller 8 (BOST device) may then be coupled to BIST circuit 7(semiconductor device), for example, through contact points 4D (e.g. probe contact pads) (first contactor) on IC 2A (wafer). (Col. 5, lines 20-24, 66,67, col. 6, line 1).

Claim 11:

Kraus teaches the functions of core wrappers 24, glue logic 36 and BIST controller 68 of FIG. 8 can be implemented by a built off-chip self test (BOST) circuit 67 (BOST device) as an integrated circuit mounted on load board 66. Kraus also teaches the core wrapper 24 includes a tester circuit 40 which also includes a pattern generator 50 (all part of the BOST device) clocked by the CLOCK signal for generating data, address and control data patterns supplied as inputs to RAM 12 via multiplexers 42-44 during a RAM test. Kraus further discloses pattern generator 50 (pattern generating circuit) includes a data generator 70 clocked by a DATA CLOCK signal from a sequencer 72 (generates clock) for producing the data pattern to be placed on the data input lines (DI) of RAM 12 (see FIG. 6). (Col. 12, lines 12-14, Col. 15, lines 40-57). Kraus further teaches an external BIST controller 8 (BOST device) may then be coupled to BIST circuit 7(semiconductor device), for example, through contact points 4D (e.g. probe contact pads) on IC 2A (second interconnection). (Col. 5, lines 66,67, col. 6, line 1).

Claim 12:

Kraus teaches a skew circuit 81 (decision circuit includes a measuring circuit) adjustably delays (measuring and access time) each of the DI, ADDR and CNT outputs of data generator 60, filters 78 and 80, and sequencer 72 with delays controlled by the SKEW data input from JTAG register 55 of FIG. 6. The delays are set to accommodate the timing requirements of the RAM under test.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al. (US-6587979), hereinafter Kraus.

Claim 10:

Kraus teaches BIST circuit 7 (semiconductor device) communicates with a BIST controller circuit 8 (BOST device) which, as illustrated in FIG. 3A, may be implemented by a separate IC mounted on the same circuit board (load board 9) (a contactor substrate for connecting the BOST device to the semiconductor device) on which IC 2A is mounted. Kraus further teaches an external BIST controller 8 (BOST device) may then be coupled to BIST circuit 7(semiconductor device), for example, through contact points 4D (e.g. probe contact pads) on IC 2A (wafer). (Col. 5, lines 20-24, 66,67, col. 6, line 1). Kraus does not explicitly teach "a socket retaining the BOST device. It would have been obvious to one of ordinary skill in the art at the time the invention was made that implementing a BIST controller circuit 8 (BOST device) as a separate IC and mounting it on the same load as the BIST circuit 7 (semiconductor device) would require a socket. The artisan would have been motivated to do so because this would enable Kraus to interchange a BIST controller with a BOST device as the testing needs of the semiconductor device require.

5. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al. (US-6587979), hereinafter Kraus, in view of Leas et al. (US-5600257), hereinafter Leas.

Claim 4:

Kraus does not explicitly teach "the external tester unit provides the BOST device with an output level generating voltage". However, Leas teaches test chip 32 (BOST device) includes controllable voltage regulator circuit 140 which is both gated and variable. Leas also teaches regulator circuit 140 is configured to receive a reference signal voltage (output level voltage) at pad 89a directly from test apparatus 58 (external test unit) (shown in FIG. 2) through reference signal line 89b. Leas further teaches the reference signal voltage is used to set the regulated output voltage level desired from voltage regulator circuit 140 (determine an input level). (Col. 9, lines 5-26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kraus's BIST controller 8 (BOST device) to include Leas's voltage regulator circuit 140. The artisan would have been motivated to do so because it would enable Kraus to control the reference voltage signal level to supply proper signal levels to the semiconductor device during testing.

Claim 7:

Kraus teaches an external BIST controller 8 (BOST device) may then be coupled to BIST circuit 7(semiconductor device), for example, through contact points 4D (e.g. probe contact pads) on IC 2A (contactor substrate). (Col. 5, lines 66,67, col. 6, line 1). Kraus does not explicitly teach "a switch circuit for disconnecting the BIST controller

8 (BOST device) from the BIST circuit 7(semiconductor device). However, Leas teaches that test signals are distributed to test chips along the surface of test wafer 30, preferably in the region between test chips 32. leas further illustrates in FIG. 3b, signal I/O lines are received on test chip pads 86a of test chips 32 (BOST device) and switches 84 (switch circuit) are provided on test chips 32 (BOST device) to disconnect test signals from a product chip (semiconductor device). (Col. 8, lines 46-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kraus's BIST controller 8 (BOST device) to include Leas's switches 84 (switch circuit). The artisan would have been motivated to do so because this would enable Kraus to disconnect test signals from a semiconductor device having a shorted I/O or other short. In addition, I/O can also be disconnected from semiconductor devices that are otherwise disconnected from power to avoid dragging down a common I/O line.

Allowable Subject Matter

6. The following is an Examiner's Statement of Reasons for Allowance:

The prior arts of record teach a test apparatus for testing a semiconductor device that comprises of and external test unit, a BIST circuit and a BOST circuit coupled between the external test unit and a BIST circuit. The prior arts of record also teach a skew circuit 81 (decision circuit includes a measuring circuit) for adjusting delays (measuring and access time) of various signals in the semiconductor device; Kraus et al. (US-6587979) is one example of such prior arts. The prior arts of record, however, fail to teach, singly or in combination, that the measuring circuit includes a logic circuit

which performs a EOR operation on the clock signal and the output signal from the semiconductor device and a frequency counter (claim 13). The prior arts of record also fail to teach, singly or in combination, that the measuring circuit further includes an OR circuit, an AND circuit, a first frequency counter, a second frequency counter, and an access-time measuring circuit (claim 14).

Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr. 6/17/05
Examiner
Art Unit 2133

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